FIG.1

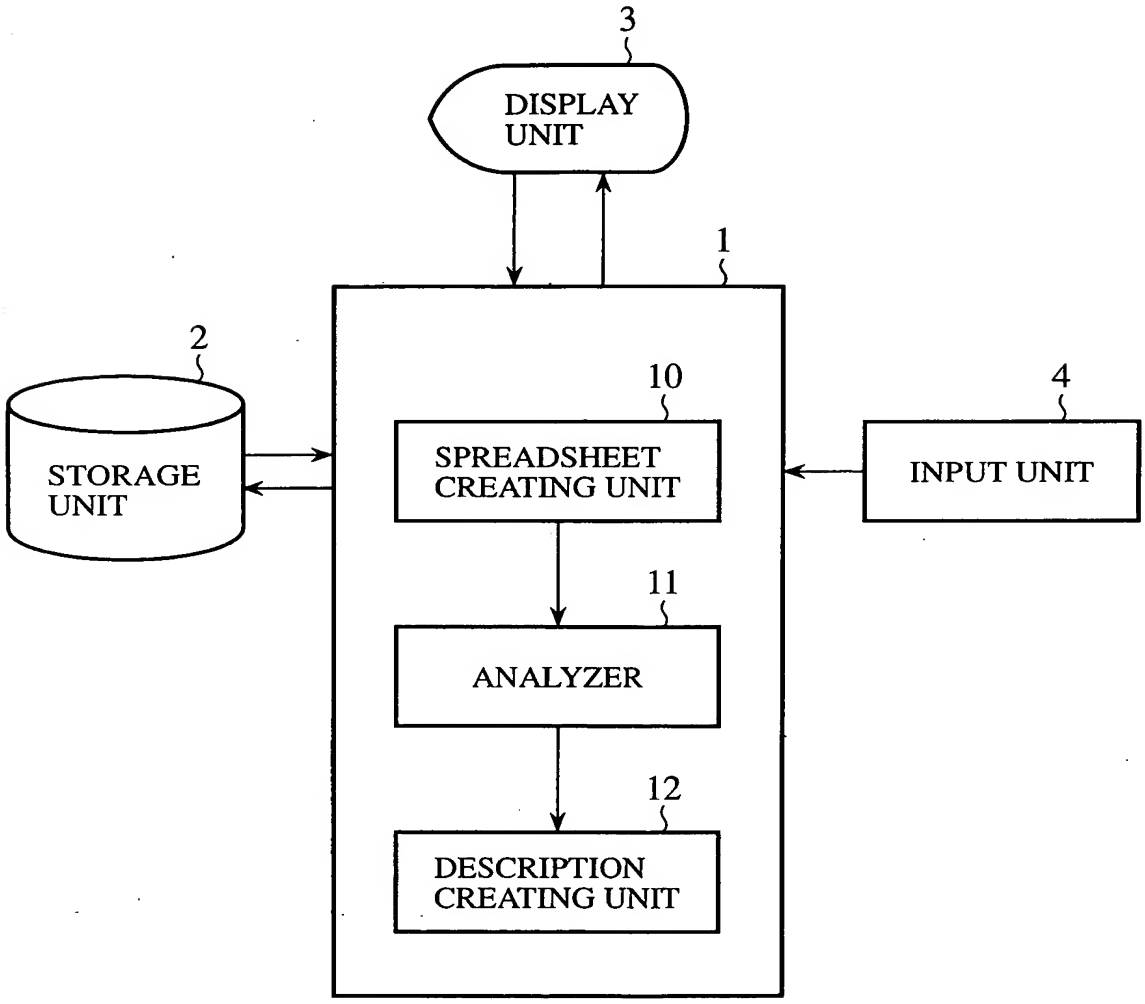
3
DISPLAY UNIT
1
2
STORAGE UNIT
10
SPREADSHEET CREATING UNIT
4
INPUT UNIT
11
ANALYZER
12
DESCRIPTION CREATING UNIT

FIG.2

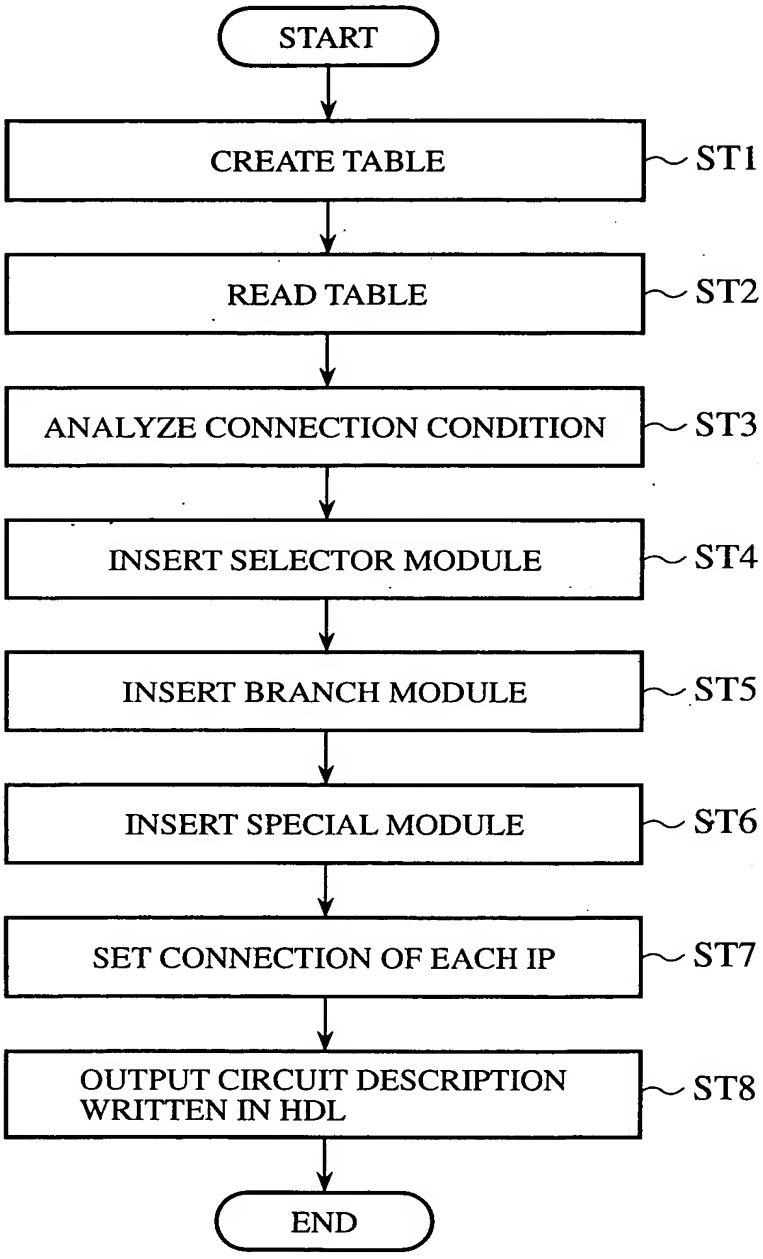
START
CREATE TABLE
ST1
READ TABLE
ST2
ANALYZE CONNECTION CONDITION
ST3
INSERT SELECTOR MODULE
ST4
INSERT BRANCH MODULE
ST5
INSERT SPECIAL MODULE
ST6
SET CONNECTION OF EACH IP
ST7
OUTPUT CIRCUIT DESCRIPTION WRITTEN IN HDL
ST8
END

FIG.3

PIN NAME	CONNECTION CONDITION 1	CONNECTION CONDITION 2	CONNECTION CONDITION 3
PA	IPA1	IPB1	IPC1
PB	IPA2	IPA2	IPA2
PC	IPA3	IPB2	IPC2
PD	IPA4	IPA4	IPC3

FIG.4

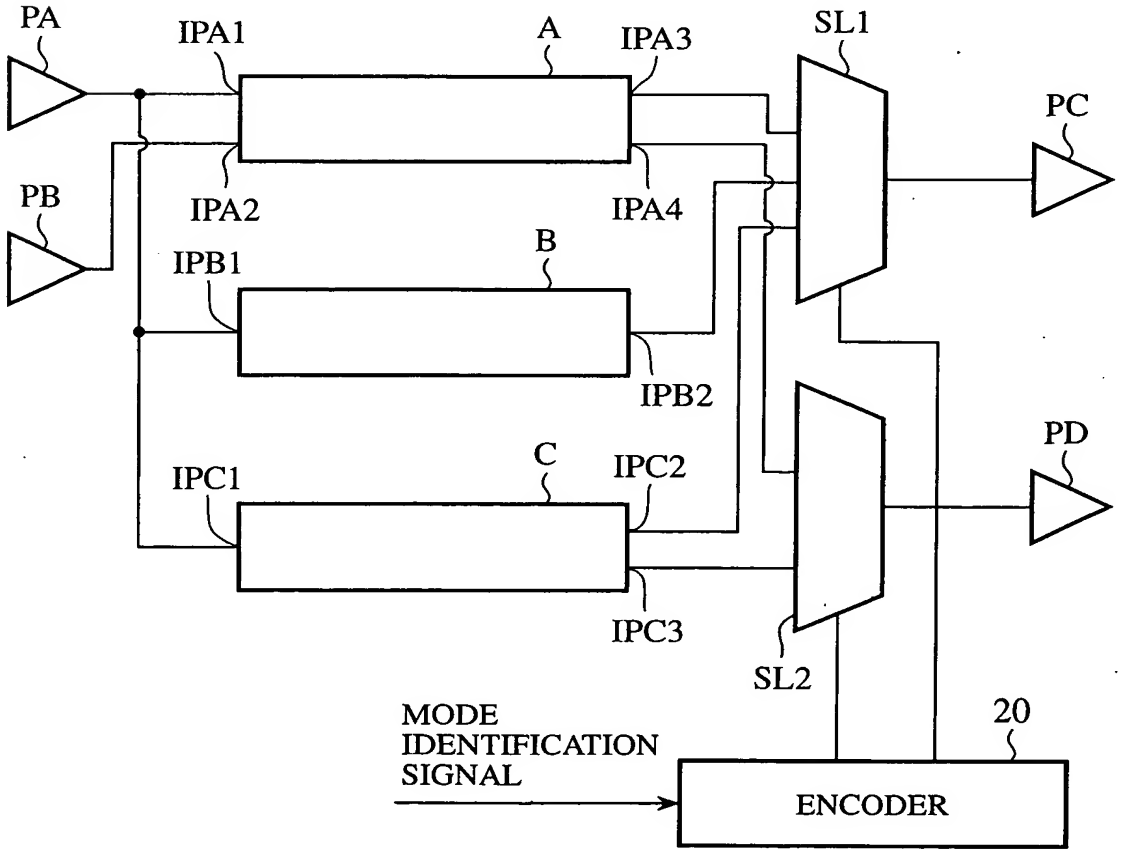

FIG.5

```
module TOP (PA, PB, PC, PD);
    input PA, PB;
    output PC, PD;
    if (CONNECTION CONDITION 1 == 1'b1) begin
      assign PA: = IPA1;
```

FIG.6

FIG.7

```
if (CONDITION LOGICAL EXPRESSION 1)
        MODE IDENTIFICATION SIGNAL 1 = ACTIVE
else
        MODE IDENTIFICATION SIGNAL 1 = INACTIVE
end
if (CONDITION LOGICAL EXPRESSION 2)
        MODE IDENTIFICATION SIGNAL 2 = ACTIVE
else
        MODE IDENTIFICATION SIGNAL 2 = INACTIVE
end
```

FIG.8

PIN NAME	NORMAL USE MODE	TEST MODE 1	TEST MODE 2	TEST MODE 3

FIG.9

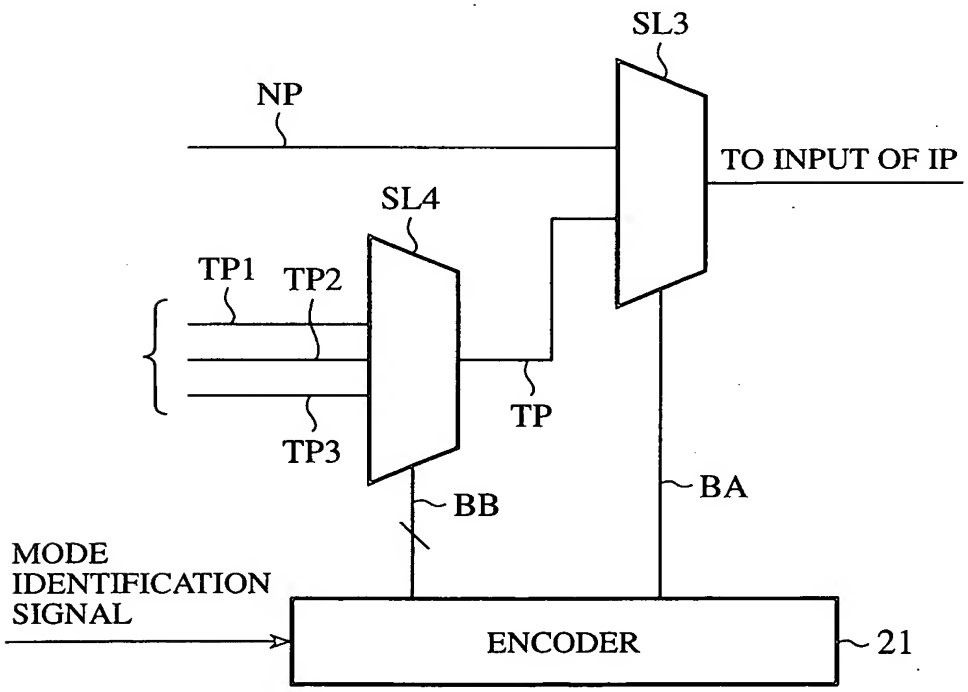

FIG.10

```
if (BA == 1)
        INPUT OF IP = NP
else
        INPUT OF IP =  OUTPUT OF SELECTOR MODULE SL4
end
if (BB == 1)
        OUTPUT OF SELECTOR MODULE SL4 = TEST PATH TP1
 else if (BB == 2)
        OUTPUT OF SELECTOR MODULE SL4 = TEST PATH TP2
 else
        OUTPUT OF SELECTOR MODULE SL4 = TEST PATH TP3
end
```

FIG.11

```
if (MODE IDENTIFICATION SIGNAL 1 == 1)
        BA = SELECTION OF NORMAL PATH
        BB = SELECTION OF TEST PATH TP1
else if (MODE IDENTIFICATION SIGNAL 2 == 1)
        BA = SELECTION OF TEST PATH
        BB = SELECTION OF TEST PATH TP1
else if (MODE IDENTIFICATION SIGNAL 3 == 1)
        BA = SELECTION OF TEST PATH
        BB = SELECTION OF TEST PATH TP2
else
        BA = SELECTION OF TEST PATH
        BB = SELECTION OF TEST PATH TP3
end
```

FIG.12

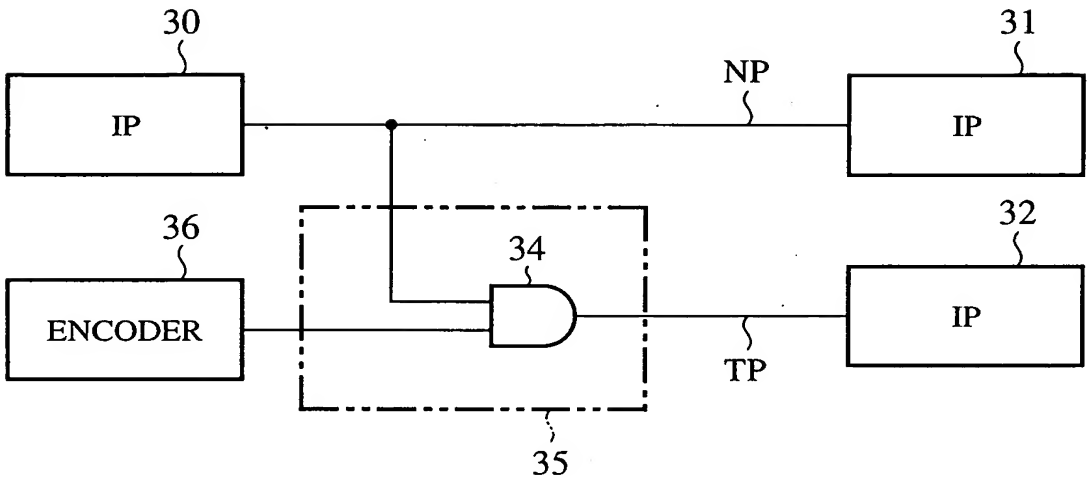

FIG.13

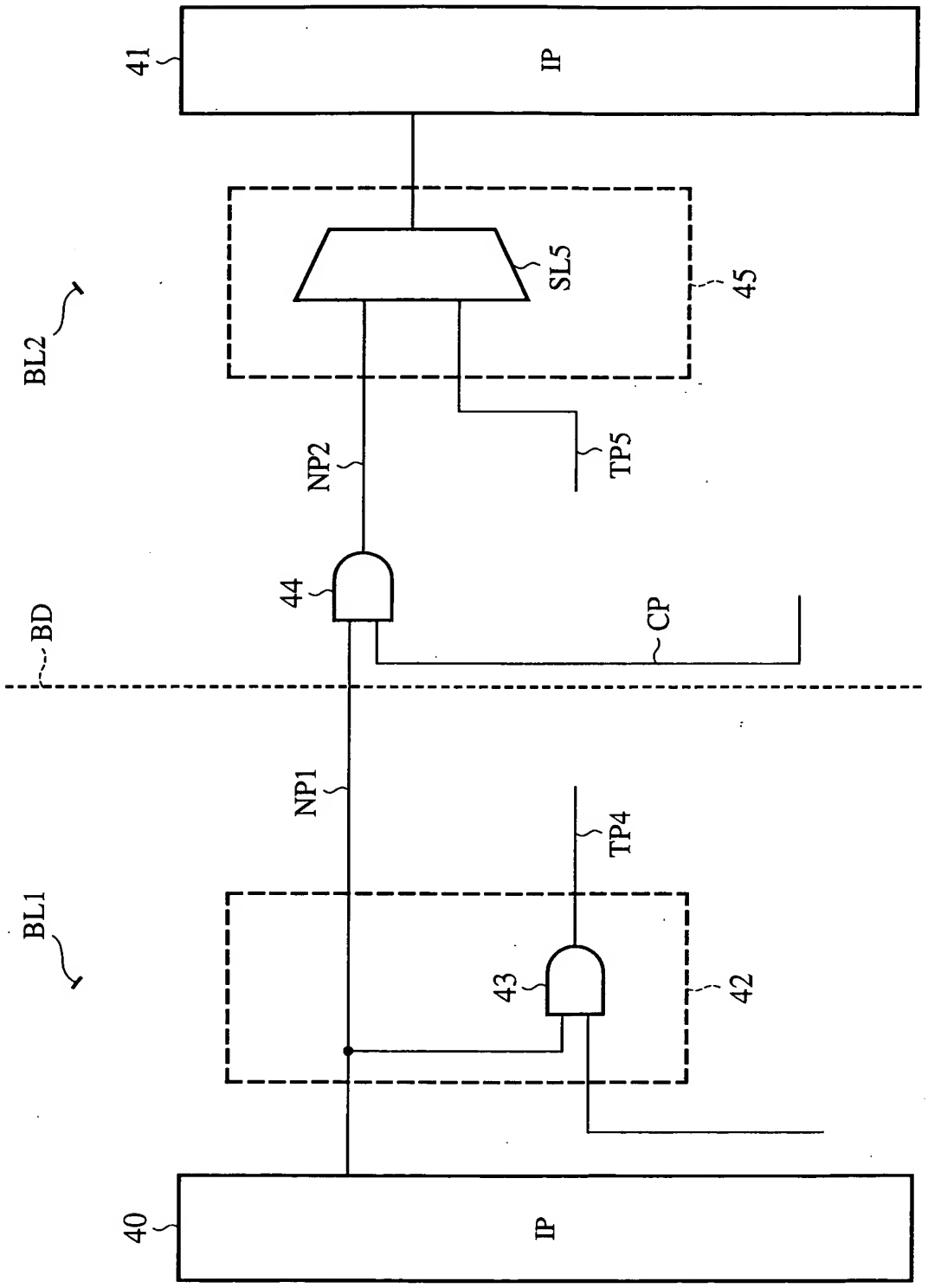

FIG.14

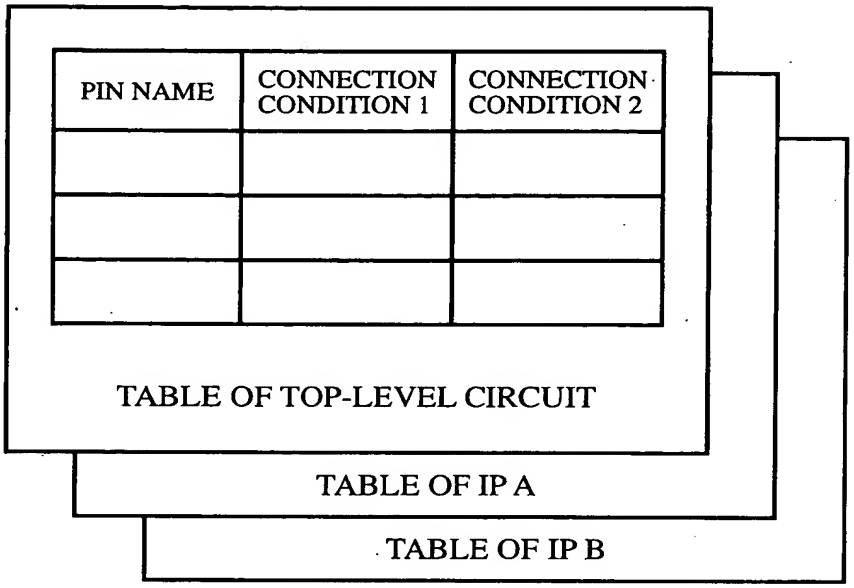
PIN NAME
CONNECTION CONDITION 1
CONNECTION CONDITION 2
TABLE OF TOP-LEVEL CIRCUIT
TABLE OF IP A
TABLE OF IP B

FIG.15

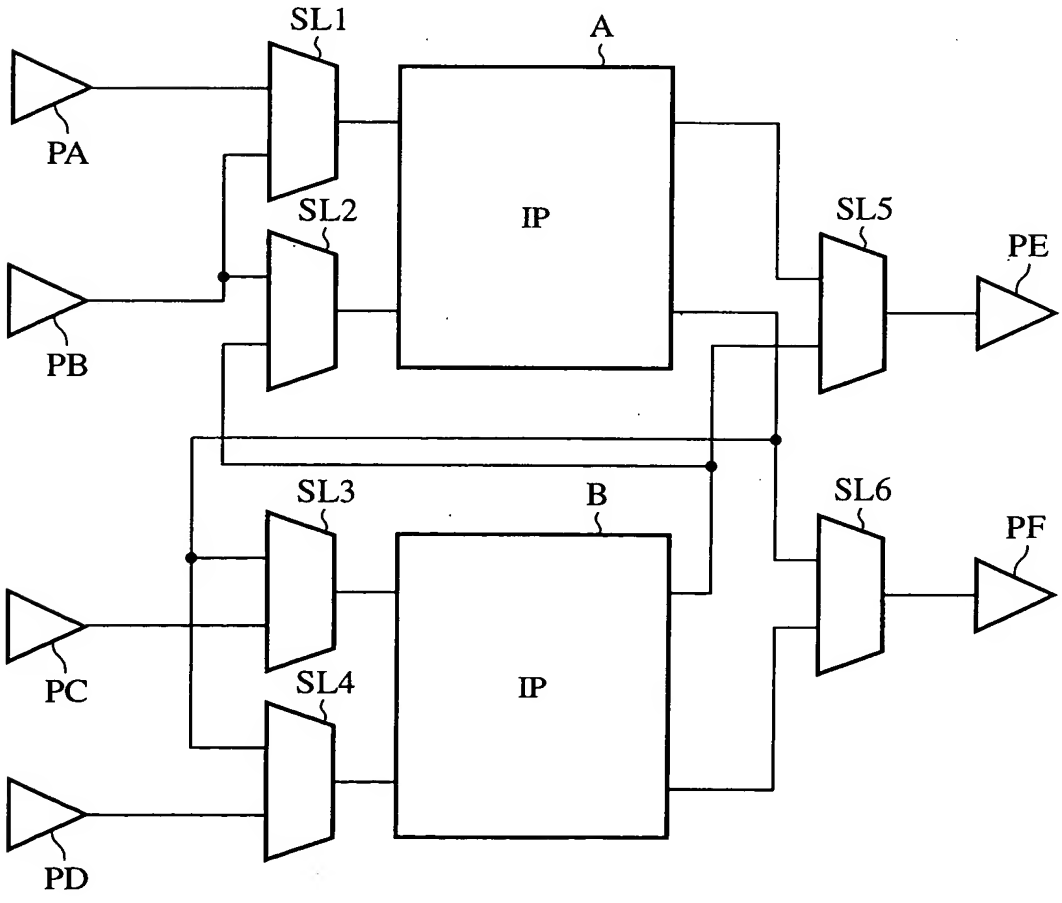
SL1
A
PA
SL2
IP
SL5
PE
PB
SL3
B
SL6
PF
PC
SL4
IP
PD

FIG.16

POWER SUPPLY GROUP	A	ON

MODE SETTING PIN		
PAD	T1	
PAD	T2	
PAD	C	
BLOCK		
PIN	IO	Default
A	Y	HUDS100LP
B	A	L4
↑	Y	U200
↑	C	L
↑	IE	L
C	A	H4
↑	Y	U200
↑	C	L
↑	IE	L
D	Y	L
E	Y	L
↑	↑	↑
F	A	L4
↑	Y	D200
↑	C	L
↑	IE	L
G	A	H4
↑	Y	D200
↑	C	L
↑	IE	L
H	A	L2
T1	Y	L
T2	Y	L

NORMAL MODE SETTING			A CUTTING OUT MODE SETTING			B CUTTING OUT MODE SETTING			C CUTTING OUT MODE 1 SETTING			C CUTTING OUT MODE 2 SETTING		
0			0			1			1			1		
0			1			0			1			1		
-			-			-			0			1		
IP	PIN(IP)	IO	IP	PIN(IP)	IO	IP	PIN(IP)	IO	IP	PIN(IP)	IO	IP	PIN(IP)	IO
A	b	I	A	b	I	B	a	I	C	a	I	C	a	I
L	-	-	L	-	-	L	-	-	C	b	O	C	b	O
A	a	I	A	a	I	-	-	-	-	-	-	-	-	-
H	-	-	H	-	-	H	-	-	L	-	-	L	-	-
H	-	-	H	-	-	H	-	-	L	-	-	L	-	-
L	-	-	L	-	-	L	-	-	L	-	-	L	-	-
A	c	I	A	c	I	-	-	-	MODE	subT	I	MODE	subT	I
H	-	-	H	-	-	L	-	-	L	-	-	L	-	-
H	-	-	H	-	-	L	-	-	L	-	-	L	-	-
C	c	I	A	g	I	B	c	I	C	c	I	C	c	I
C	d	I	A	h	I	B	b	I	C	d	I	C	d	I
A	h	I	-	-	-	-	-	-	-	-	-	-	-	-
B	e	O	A	d	O	B	e	O	C	g	O	C	g	O
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
A	FCL	O	L	-	-	L	-	-	L	-	-	L	-	-
A	FCL	O	L	-	-	L	-	-	L	-	-	L	-	-
B	d	O	A	e	O	B	d	O	L	-	-	L	-	-
-	-	-	-	-	-	-	-	-	C	f	I	C	f	I
L	-	-	L	-	-	L	-	-	H	-	-	H	-	-
L	-	-	L	-	-	L	-	-	H	-	-	H	-	-
C	e	O	A	f	O	B	f	O	C	e	O	C	e	O
MODE	t1	I	MODE	t1	I	MODE	t1	I	MODE	t1	I	MODE	t1	I
MODE	t2	I	MODE	t2	I	MODE	t2	I	MODE	t2	I	MODE	t2	I

FIG.17

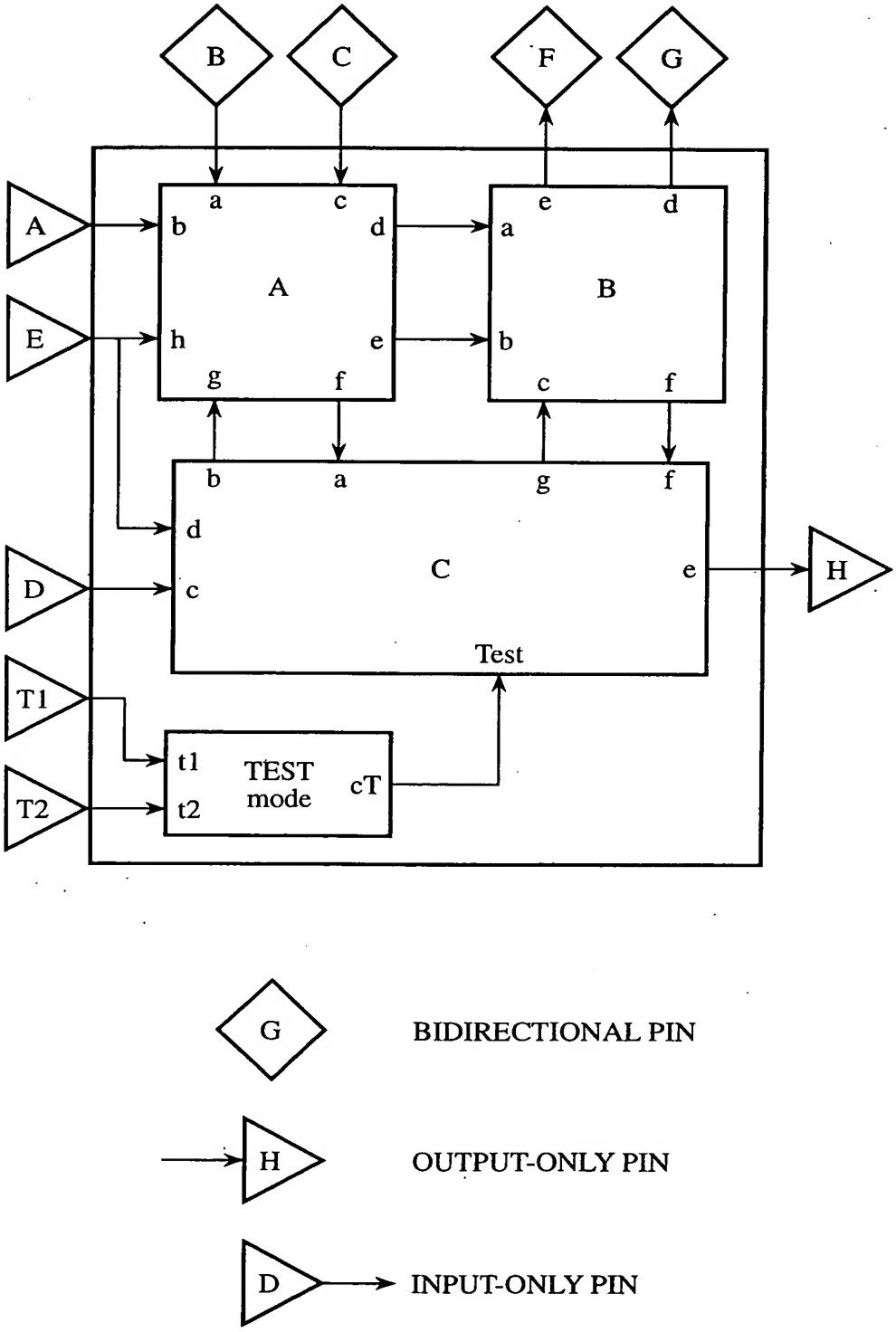
B
C
F
G
A
E
D
T1
T2
H
a
b
c
d
e
f
g
h
A
B
C
Test
t1
t2
TEST
mode
cT
BIDIRECTIONAL PIN
OUTPUT-ONLY PIN
INPUT-ONLY PIN

FIG.18

POWER SUPPLY GROUP	B	ON-OFF

MODE SETTING PIN		
PAD	T1	
PAD	T2	
PAD	C	
BLOCK		
PIN	IO	Default
a	I	L
b	I	H
c	I	L
d	O	-
e	O	-
f	O	-
g	I	H
FLC	O	-
h	I	L

NORMAL MODE SETTING			A CUTTING OUT MODE SETTING			B CUTTING OUT MODE SETTING			C CUTTING OUT MODE 1 SETTING			C CUTTING OUT MODE 2 SETTING		
0			0			1			1			1		
0			1			0			1			1		
-			-			-			0			1		
IP	PIN(IP)	IO	IP	PIN(IP)	IO	IP	PIN(IP)	IO	IP	PIN(IP)	IO	IP	PIN(IP)	IO
PAD	B	I	PAD	B	I	L	-	-	L	-	-	L	-	-
PAD	A	I	PAD	A	I	L	-	-	L	-	-	L	-	-
PAD	C	I	PAD	C	I	L	-	-	L	-	-	L	-	-
B	a	O	PAD	F	O	-	-	-	-	-	-	-	-	-
B	b	O	PAD	G	O	-	-	-	-	-	-	-	-	-
C	a	O	PAD	H	O	-	-	-	-	-	-	-	-	-
C	b	I	PAD	D	I	L	-	-	L	-	-	L	-	-
PAD	F	O	-	-	-	-	-	-	-	-	-	-	-	-
PAD	E	I	PAD	E	I	L	-	-	L	-	-	L	-	-

FIG.19

POWER SUPPLY GROUP	B	ON-OFF

MODE SETTING PIN		
PAD	T1	
PAD	T2	
PAD	C	
BLOCK		
PIN	IO	Default
e	O	-
d	O	-
a	I	L
b	I	H
c	I	L
f	O	-

NORMAL MODE SETTING			A CUTTING OUT MODE SETTING			B CUTTING OUT MODE SETTING			C CUTTING OUT MODE 1 SETTING			C CUTTING OUT MODE 2 SETTING		
0			0			1			1			1		
0			1			0			1			1		
-			-			-			0			1		
IP	PIN(IP)	IO	IP	PIN(IP)	IO	IP	PIN(IP)	IO	IP	PIN(IP)	IO	IP	PIN(IP)	IO
PAD	F	O	-	-	-	PAD	F	O	-	-	-	-	-	-
PAD	G	O	-	-	-	PAD	G	O	-	-	-	-	-	-
A	d	I	L	-	-	PAD	A	I	L	-	-	L	-	-
A	e	I	L	-	-	PAD	E	I	L	-	-	L	-	-
C	g	I	-	-	*	PAD	D	I	-	-	*	-	-	*
C	f	O	-	-	-	PAD	H	O	-	-	-	-	-	-

FIG.20

POWER SUPPLY GROUP	A	ON

MODE SETTING PIN		
PAD	T1	
PAD	T2	
PAD	C	
BLOCK		
PIN	IO	Default
d	I	L
c	I	H
e	O	-
a	I	L
b	O	-
f	I	L
g	O	-
test	I	L
PCA	O	-
PCB	O	-

NORMAL MODE SETTING			A CUTTING OUT MODE SETTING			B CUTTING OUT MODE SETTING			C CUTTING OUT MODE 1 SETTING			C CUTTING OUT MODE 2 SETTING		
0			0			1			1			1		
0			1			0			1			1		
-			-			-			0			1		
IP	PIN(IP)	IO	IP	PIN(IP)	IO	IP	PIN(IP)	IO	IP	PIN(IP)	IO	IP	PIN(IP)	IO
PAD	E	I	L	-	-	L	-	-	PAD	E	I	PAD	E	I
PAD	D	I	L	-	-	L	-	-	PAD	D	I	PAD	D	I
PAD	H	O	-	-	-	-	-	-	PAD	H	O	PAD	H	O
A	f	I	H	-	-	H	-	-	PAD	A	I	PAD	A	I
A	g	O	-	-	-	-	-	-	PAD	B	O	PAD	B	O
B	f	I	-	-	*	-	-	*	PAD	G	I	PAD	G	I
B	c	O	-	-	-	-	-	-	PAD	F	O	PAD	F	O
MODE	cT	I	MODE	cT	I	MODE	cT	I	MODE	cT	I	MODE	cT	I
MODE	AtoC	O	MODE	AtoC	O	MODE	AtoC	O	MODE	AtoC	O	MODE	AtoC	O
MODE	BtoC	O	MODE	BtoC	O	MODE	BtoC	O	MODE	BtoC	O	MODE	BtoC	O

Title: AUTOMATIC CIRCUIT DESIGN APPARATUS AND COMPUTER-IMPLEMENTED AUTOMATIC CIRCUIT DESIGN METHOD
Inventors: NAGASAWA et al.
Atty Docket No.: 402924
Leydig, Voit & Mayer 202-737-6770